AMENDMENTS TO THE CLAIMS

This listing of claims replaces all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS

1. (cancelled)

2. (cancelled)

3. (cancelled)

4. (cancelled)

5. (cancelled)

6. (cancelled)

7. (cancelled)

8. (cancelled)

9. (cancelled)

10. (cancelled)

11. (cancelled)

12. (cancelled)

13. (cancelled)

14. (original) A method for regulating gate oxide layer formation, comprising:

defining a wafer as a plurality of portions;

establishing one or more gate oxide layer formations to be formed;

directing light onto at least one of the gate oxide layer formations;

collecting light reflected from at least one gate oxide layer formation;

analyzing the reflected light to determine thickness and/or uniformity of the at least one gate oxide layer formation; and

controlling one or more gate oxide layer formers to regulate gate oxide formation of the at least one gate oxide layer formation.

15. (original) The method of claim 14, wherein analyzing the reflected light further comprises:

employing a scatterometry system to process the reflected light.

16. (original) The method of claim 14, where the gate oxide layer is a high K material.

17. (original) The method of claim 14, where the gate oxide layer is a metal oxide.

18. (original) The method of claim 14, further comprising:

using a processor to control the at least one gate oxide former based at least partially on data received from the scatterometry system.

19. (original) The method of claim 18, further comprising:

using a processor to control the at least one gate oxide former based at least partially on data received from the scatterometry system.

20. (original) A method for regulating gate oxide layer formation, comprising:

partitioning a wafer into a plurality of grid blocks;

using one or more gate oxide layer formers to form one or more gate oxide layers on the wafer, each gate oxide former functionally corresponding to a respective grid block;

determining thickness and/or uniformity of the one or more gate oxide layer formations on one or more portions of the wafer, each portion corresponding to a respective grid block; and

using a processor to coordinate control of the gate oxide layer formers, respectively, in accordance with determined gate oxide thickness and/or uniformity of the respective portions of the wafer.

21. (cancelled)

22. (new) A method for regulating gate oxide layer formation, comprising:

defining a wafer as a plurality of portions;

establishing one or more gate oxide layer formations to be formed;

directing light onto at least one of the gate oxide layer formations;

collecting light reflected from at least one gate oxide layer formation;

analyzing the reflected light to determine thickness and/or uniformity of the at least one gate oxide layer formation by using a scatterometry system to process the reflected light; and

controlling one or more gate oxide layer formers to regulate gate oxide formation of the at least one gate oxide layer formation.

23. (new) The method of claim 22, where the gate oxide layer is a high K material.

24. (new) The method of claim 22, where the gate oxide layer is a metal oxide.

25. (new) The method of claim 22, further comprising:

using a processor to control the at least one gate oxide former based at least partially on data received from the scatterometry system.

26. (new) The method of claim 25, further comprising:

using a processor to control the at least one gate oxide former based at least partially on data received from the scatterometry system.

27. (new) The method of claim 22, where the gate oxide layer has a thickness of less than about 20 nanometers.

28. (new) The method of claim 22, where the reflected light is analyzed to determine thickness of the at least one gate oxide layer formation.

29. (new) A method for regulating gate oxide layer formation, comprising:

partitioning a wafer into a plurality of grid blocks;

using one or more gate oxide layer formers to form one or more gate oxide layers on the wafer, each gate oxide former functionally corresponding to a respective grid block;

determining thickness and/or uniformity of the one or more gate oxide layer formations on one or more portions of the wafer using a scatterometry system, each portion corresponding to a respective grid block; and

using a processor to coordinate control of the gate oxide layer formers, respectively, in accordance with determined gate oxide thickness and/or uniformity of the respective portions of the wafer.

30. (new) The method of claim 29, where the gate oxide layer is a high K material.

31. (new) The method of claim 29, where the gate oxide layer is a metal oxide.

32. (new) The method of claim 29, where the gate oxide layer has a thickness of less than about 20 nanometers.

33. (new) The method of claim 29, where the thickness of the at least one gate oxide layer formation is determined.